Fenlow

161

# DIGITAL VOLTMETER
# Type 301-A - 501-A

Fenlow Electronics Ltd
SPRINGFIELD LANE
WEYBRIDGE - SURREY

# Specification

## Voltage Ranges

| | | | |
|---|---|---|---|
| Range (1) | 0 | - | 100mV |
| Range (2) | 0 | - | 1 V |
| Range (3) | 0 | - | 10 V |
| Range (4) | 0 | - | 100 V |
| Range (5) | 0 | - | 1000 V |

## Over-ranging

Over-ranging of 40% on all ranges is provided for, with overload flashing indicator when the voltage is outside the 40% over-range.

## Input Impedance

| | | |
|---|---|---|
| Range (1) | greater than | 100 Megohms |
| Range (2) | " " | 1000 Megohms |
| Range (3) | " " | 10,000 Megohms |
| Range (4) | " " | 10 Megohms |
| Range (5) | " " | 10 Megohms |

## Common Mode Resistance

Greater than 10,000 Megohms

Common mode voltages max. 500V

## Series Mode Rejection

Rejection of interference at the mains frequency (even when this deviates from its nominal 50 or 60 c.p.s.) and harmonics, without the use of filters, 70 dbs for up to 3% deviation of the mains frequency.

With filters - 100dbs rejection

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Common Mode Rejection

(Ratio between the common mode voltages and the voltage read by the DVM) at D.C. 140 dbs at 50 c.p.s. - 150 dbs with 1000ohms out of balance.

Input Offset Current

Balanced to zero by panel control, changes with temperature.

| | |
|---|---|
| Range (1) ) Range (2) ) Range (3) ) | $10^{-11}$ amps. per degree C. |
| Range (4) | $10^{-12}$ amps. per degree C. |
| Range (5) | $10^{-13}$ amps. per degree C. |

Sensitivity

| | |
|---|---|
| Range (1) | 10 microvolts |
| Range (2) | 100 microvolts |
| Range (3) | 1 millivolt |
| Range (4) | 10 millivolts |
| Range (5) | 100 millivolts |

Resolution

1 part in 14,000

Accuracy

$\pm$ 0.01% $\pm$ 1 digit

Polarity Indication

Automatic by sign indicator tube.

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## Sampling Rate

for complete information and sign

### Internal

Max. 25 samples per second, intervals of 40, 80, 160, 320, 640, and 1,280 millisecs. as set by front panel controls.

### External

Up to a maximum of 25 samples per second as demanded by interrogator pulse. Complete sign determination is carried out within the 40m sec. (The measurement is made during the mains period succeeding the interrogate pulse).

* When operated on 60 c.p.s. mains the maximum rate are 30 with proportional change in the intervals.

### Display

By nixie indicator tubes with storage to give anti blink readout. Max. reading +1400.0.

## Calibration

By means of Muirhead reference cell. Temperature coefficient 5 microvolts per degree C.

Current and voltage zero balance by front panel controls.

## Data Output

Decimal coded information, sign, range and overload by means of a 54-way connector at the rear. For any BCD output decoder units plug into the rear of the instrument. When the decoder is used the levels and signs correspond with the NPL standard interface.

## Data Levels

### Without Decoder

Decimal information +55V at 0.1ma for zero, +5V at 0.5ma for digits. Decimal point +55 to +70V at 0.5ma for the range or open circuit. Sign information +55V 0.1ma to 0.2V at 0.5ma. Overload indicator voltage and currents as for decimal point, flashing rate 640 m. sec. period. Instruction to print +8V 5.0ma 20 m. sec. pulse. Interrogate input +8V m. sec. rise time greater than 1V per microsecond.

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With Decoder

Types D.C.1 (1248 code) and D.C.2 (1224 code). All outputs, no information 0 volts, with information +11 volts, from 2.2K source impedance. Instruction to print pulse length 20m sec. Interrogate pulse +8V rise time greater than 1V per microsecond.

Calibration and Zero Balance

Provision is made for calibration and zero adjustment by means of screwdriver adjusted potentiometers on the front panel. Separate facilities are provided for positive and negative calibration. For zero balance provision has been made for both voltage and current balance, many digital voltmeters do not have this facility, because they are intended to work from low source impedances where the out of balance current is not important.

The current balance and voltage controls should be adjusted so that a change of source resistance does not shift the zero. If the source impedance is changed from zero to 1Mohms, a current of 0.1 nano amperes will give rise to 100 microvolts, which is equal to the least significant digit on the 1V range. Calibration can be carried out by switching to this range and setting the voltage adjustment to give zero when the input terminals are shorted together, and the current adjustment to give zero when 1Mohm is used as a source, repeating this procedure until zero is obtained for both conditions.

For many uses the exact current zero is not important and the zero can be set by using only the voltage control, pressing the Cal. zero button disconnects the input amplifier from the input terminals of the instrument, connects them together (zero resistance) and puts the instrument on the 100mV range, this can be used for the approximate voltage balance.

The Cal. positive and Cal. negative buttons put the instruments on the 1V range, disconnect the input amplifier from the input terminals and apply the Reference Cell of the appropriate polarity.

These adjustments should not be carried out in the presence of a large common mode voltage.

## Internal Pre-set Controls

Internal pre-set controls are available through the floating unit cover, their functions are:

### Zero Detector Zero

For setting the level at which the zero detector produces an output transition.

### Integrator Zero

For setting the integrator rate to zero for zero input.

### Signed Zero Positive and Negative

These controls alter the offset voltage and give independent control of the positive and negative zeros.

### Calibration Centralize

This control centralizes the front panel positive and negative calibration controls.

## Input Connections

Four wires are available for connecting to the input of the digital voltmeter, they are INPUT HIGH, INPUT LOW, GUARD and mains EARTH. On all the transformers used for coupling into the floating unit both primary and secondary screens are used. All the primary screens are connected to the mains EARTH and main chassis and all the secondary screens are connected to the GUARD together with the screen of the input amplifier.

The GUARD CONNECTION MUST BE CONNECTED TO EITHER THE INPUT LOW, INPUT HIGH OR SOURCE OF COMMON MODE, in the absence of common mode voltages or when the common mode voltage is between input low and mains earth, the GUARD and INPUT LOW SHOULD BE CONNECTED TOGETHER EXTERNALLY.

No damage will be caused if the guard is left free but errors can occur in certain circumstances on the most sensitive range.

## System Description

### General

The DVM type 301-A is an integrating digital voltmeter, that is, the applied voltage to be measured is integrated over a period and the output of the integrator is then determined by applying a known voltage (the reference), to reset the integrator to zero.

With many digital voltmeters the period of integration is fixed to be equal to approximately one period of the mains frequency, with a view to eliminating errors due to contamination of the input signal by the mains frequency and harmonics of it. With instruments which have fixed integration times, errors arise when the mains frequency changes from its nominal 50 or 60 c.p.s. and these errors can be very large. For example, if the interfering signal has a peak amplitude equal to say 10 times the D.C. voltage to be measured and the phase is in the most unfavourable condition, a 1% deviation of the mains period from the integration period will cause an error of 10% in the reading. This is clearly a great disadvantage in systems work where interfering signals are often present. Some integrating digital voltmeters cease to function correctly when the sign of the integration changes during the integration period.

In the DVM type 301-A the integration period is accurately locked to the mains frequency by servo controlling the oscillator using the counter and an auxiliary early and late strobe control loop. The system design is such that a reversal of sign of the integrator output during the integration period does not affect the system.

The DVM type 301-A makes use of a system which is independent of the oscillator frequency, pulses from the same source are fed into the counter during the signal period and the reference period in such a way that the final reading is independent of the oscillator frequency. Having got a system where the integration period is determined by a count from the oscillator and the measurement is independent of the oscillator frequency, it is only Necessary to control the oscillator to follow the mains frequency to completely eliminate the effects of interfering signals at the fundamental and harmonics of the mains frequency, when it changes by a few per cent. The gain in the oscillator servo control loop is such that the difference between the integration period and the mains period are reduced by a factor of 100, i.e. 1% difference is reduced to 0.01% difference and the errors due to interference are reduced accordingly. Some instruments reduce the effects of interference by the use of filters, these can be effective but only at the expense of sampling rate. Twin "T" filters, etc. would need to track the

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mains frequency to be effective enough, multi-section low pass filters are often used, in either case up to eight time constants may have to elapse before the input voltage has reached its final level, reducing the possible sampling rate to seconds. A filter has been included in the DVM type 301-A but should only be used on the slow readout positions.

The system used in the DVM is simple in principle but because many elements have multiple purposes it is difficult to describe by starting with a complete system diagram. To avoid confusion the system will be described in parts with the aid of simplified schematics, and then the system as a whole will be described with the aid of the master timing waveform diagram. Parts of the DVM are floating to facilitate differential operation in the presence of common mode voltages. The input amplifier, integrator, reference system, the reference logic and sign logic are all in the floating unit, coupling to this unit is made by transformers. Some of the bistables used in the logic are duplicated in the floating and grounded units.

The detail of those parts which are floating and those which are grounded will be omitted in the early parts of this description.

The system can be best described by splitting it into the following parts

1) Input Amplifier

2) Integrator and Switching Systems

3) Oscillator Control Loop

4) Counter and Readout Unit

5) Programme Unit

Input Amplifier (General Description)

The purpose of the input amplifier is to scale input signals to a suitable level for integration, and to provide a very high input impedance to prevent loading of the input attenuator, and to prevent loading the source on the lower voltage ranges. A schematic diagram showing the method of connection for this amplifier is shown in Fig.1. The method of connection for the amplifier produces an effective input resistance between terminals (1) and (2) which is equal to R multiplied by the loop gain, the forward gain of the amplifier is made high enough to make the loading on the input attenuator negligible. With the method of connection used the gain is determined by the ratio $(R_2 + R_1)/R_1$.

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On the 100V and 1000V ranges the amplifier has a gain of 2 and the range change is carried out by altering the lower resistance in the input attenuator. On the 10V, 1V and 100mV ranges the input attenuator is omitted and the range change is carried out by alteration of the values of $R_2$ and $R_1$. On the 10V range the amplifier has a gain of 2, on the 1V range a gain of 20 and on the 100mV range a gain of 200.

As will be seen from Fig.1 there is no common connection between the input and output of the amplifier but since the outputs feed into a unit which is completely floating there is no disadvantage in this. The main properties required from this amplifier are that it should have low drift and zero or an extremely low current flowing back to the source. It should also have an input impedance which is extremely high and it should be linear. Both the last properties improve with the excess gain. Full details of these properties are given in the Input Amplifier detail description in a later chapter.

Integrator and Switching (General)

Fig.2 shows the basic parts of the measuring system used. Measurement of the unknown voltages (signal) is carried out by applying the signal to the integrator input for a length of time determined by a number of oscillator pulses (10,000 pulses at approximately 500K c.p.s., this being controlled by a separate loop so that 10,000 pulses equal to 1 mains period). The counter is initially set so that when 10,000 pulses have been applied an output is obtained which switches off the signal and applies the reference. According to the sign of the input, the reference sign must be changed to cause the integrator output to fall linearly to zero. The sign of the reference which is applied is obtained by the sign of the output at the end of the integration period as indicated by the state of the sign detector amplifier, this level is used in the control logic to apply the appropriate reference sign. The magnitude of the applied input voltage is obtained by the count of the number of pulses from the oscillator passing into the counter during the reference period, (during this period pulses directly from the oscillator at 1M c.p.s. are used, this is simply to save time. The reference voltage being appropriately scaled to 2 : 1).

As will be seen the accuracy of the measurement is determined by the integrating resistors, the reference accuracy and the amplifier gain and linearity but is independent of the oscillator frequency and the value of the integrating capacitor. The diagram of Fig.2 indicates only the general principle of the operation and does not include several details which are necessary in the practical system. The main points are that the initiation of the integration period is obtained from the mains waveform (but

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the particular point is unimportant), the signal period is terminated by a pulse from the counter after a given number of oscillator pulses and the reference with appropriate sign is applied at this point, termination of the reference period is by a pulse from the zero detector and the level of the signal voltage is obtained by the count during the reference period.

Oscillator Control Loop (General)

The control of the integration period to be equal to one mains period is carried out by an early and late strobe control loop similar to the arrangement often used in automatic radar tracking.

Diagrams of the system and timing waveforms are shown in Fig. 3 and Fig. 3A respectively. The trailing edge of monostable B which is triggered by the mains driven Schmitt trigger circuit and passed via an "and" gate which eliminates alternate pulses, opens the oscillator gate and allows pulses from the oscillator divider circuit into the counter. (This is the interval during which the signal voltage is being applied to the integrator). 200 microseconds or 100 pulses before the counter reaches a count of 10,000 a pulse is obtained from the counter which is used to trigger a 400 microsecond monostable, the output waveform from this monostable is fed into two gates together with waveforms from the early and late monostables. The early monostable, monostable B, is triggered every mains period and an "and" gate with an input from the divide by 2 circuit eliminates alternate monostable B pulses. The trailing edge of this "and" gate triggers the late monostable. The early and late monostables provide inputs to the strobe gates on alternate mains periods. The trailing edge of the above "and" gate waveform will correspond to exactly 10,000 pulses if the oscillator frequency is exactly 20,000 times the mains frequency. The control loop formed by taking the error from the early and late strobe gates controls the oscillator to be 20,000 times the mains frequency, and hence a count of 10,000 pulses to correspond to one mains period. The control loop gain, etc. has been chosen to correct the errors to within a few microseconds. It is important to note that the system accuracy does not depend upon this control, it is only introduced to remove the effects of spurious series mode signals.

Counter and Readout Unit (General)

The DVM type 301-A makes use of a decimal counting system with auxiliary storage facilities. With both internal and external triggering the counter is reset every 40m sec. and new information is measured on the counter every 40m sec. The transfer to store is carried out at a rate determined by the setting of the readout rate switches which are multiples of 40m sec. In the case of external programming the transfer to store rate and the rate at which data

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is presented on the output terminals is determined by the rate of interrogation, in this case the data and the instruction to print are provided after the next complete mains cycle following the interrogate pulse.

Pulses are taken from the counting chain for various internal purposes.

1) A pulse to work the centre strobe in the oscillator control loop.

2) A pulse after 10,000 counts to terminate the signal input period (Offset start pulse).

3) A pulse to terminate an offset voltage (not previously mentioned).

4) In overload conditions pulses are taken from the counter to initiate the warning indicator.

The Programme Unit (General)

The purpose of the programme control unit is to enable the DVM to be interrogated by external pulses and for it to provide instruction to print information when the data is available.

In the case of internal operation the programme unit simply provides a print pulse at a suitable time and a rate as set by the readout rate controls on the front panel, with a maximum rate of 25 per second.

When the DVM is being interrogated the programme unit ensures that the DVM will take the next complete mains period after the interrogation as the measuring time and it again gives an instruction to print when the data is available. Both on internal and external working the DVM measures the input quantity every 40m sec. and since the external interrogate pulse could occur during a measuring period it is important that the programme unit holds the interrogate pulse until the start of the next complete measuring interval. The maximum permissible interrogation rate is 25 per second. A diagram showing the timing of the interrogation pulse and print out pulse is given in Fig. 4 .

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## Technical Description

### Control System

### Integrator Switching, Reference Switching, Oscillator Control Loop and Readout Systems

The system will first be described with reference only to the timing diagram Fig.5, we will explain what triggers what but not show how. Having done this it will be strightforward to describe the system block diagram.

To facilitate control of the oscillator by the strobe servo loop making use of the existing counter, it is necessary to start the measurement period by a pulse derived from the mains waveform. Before the measurement interval commences the previous data must be transferred to the store and the counter reset, the mains waveform is used to trigger these pre pulses before the measurement interval is commenced.

Referring to the timing waveform diagram Fig.5 the top waveform (1) is the mains waveform. Waveform (2) is the Schmitt trigger waveform derived from the mains input. The Schmitt trigger waveform drives a binary counting chain which is used to trigger the transfer to store pulse former (29) which gives the readout rate. The first stage of the divider chain produces waveform (3) which is used in many places in the logic to eliminate alternate pulses, hence the term selector gating bistable.

The edges of the Schmitt trigger waveform are used to trigger a 1m sec. monostable, the "delay reset monostable ", the waveform is shown in (5).

The trailing edge of the "delay reset monostable" triggers another monostable 2.5m sec. in length, this waveform (6) is used for resetting the counter on one set of alternate mains periods and as the early strobe gate for the oscillator control system on the other alternate mains periods. Alternate trailing edges of this waveform are used to trigger the "signal bistable" and the "integrate bistable" to start the integration period. The trailing edge of the pulse is gated by (3) as shown in (7), the signal bistable is shown in (11) and the integrate bistable in (18).

The signal bistable does two things, it switches the signal input into the integrator and also opens a gate allowing pulses from the oscillator at 10,000 times the mains frequency into the counter.

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When 9900 pulses have been fed into the counter a pulse (8) is given out which is used to initiate the centre strobe for the oscillator control this is the 0.4m sec. monostable shown in (25).

After 10,000 pulses have been fed into the counter another pulse (9) is obtained which switches off the signal bistable (11) removing the signal from the integrator. At this time the offset voltage either positive or negative according to the sign of the input is fed into the integrator, the waveforms are shown in (14) and (15). (The purpose of this offset will be explained later). The termination of the offset pulse is by a pulse from the counter when 10970 pulses have been fed in. The pulses fed to the counter during the signal period are at 10,000 times the mains frequency and during the offset and reference period they are at 20,000 times the mains frequency.

The termination of the offset period corresponds to the start of the reference period. The sign of the applied reference is determined by the sign of the output from the zero detector at the end of the signal integration period.

When the integrator output voltages reaches zero a pulse is given out by the zero detector circuit, this is shown by waveform (12). This pulse switches off the integrate bistable and removes the references.

During the time that the reference is being applied to the integrator, pulses at a frequency 20,000 times the mains frequency are fed into the counter. The number of pulses fed in during this time is a measure of the input voltage.

Voltage Offset System

Without any voltage offset the triangle ABC of waveform (19) would shrink to zero for zero input signal. There are practical difficulties in measuring the time BC when it becomes very small.

To avoid these problems, a small offset voltage is applied to the integrator after the signal integration period. The sign of the offset is arranged to be the same as the signal input by using "and" gates which have a sign dependent inputs derived from the zero detector amplifier. The effect of this offset is to give non zero values for AB and CD of waveform (19) when zero input is applied. The levels are arranged so that the offset corresponds to 30 least significant digits. Having explained the offset we can now consider the initial setting of the counter, etc.

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Initial Counter Setting

The counter is initially set by the reset pulse to 09000 when 11000 pulses have been applied - 10,000 during the signal integrate period at 10,000 times the mains frequency, and 970 during the offset period and 30 during the reference period at 20,000 times the mains frequency, the counter will read 00000. Higher counts give the correct indication of the voltage.

Since the counter is initially set to 09000 the pulse which initiates the centre strobe after 9900 pulses is when the counter reading is 18900. The pulse which terminates the signal period after 10,000 input pulses is when the counter reading is 19000.

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GROUNDED LOGIC

List of "and" gates used on DVM type 301-A

Integrator Discharge Gate

This gate produces a pulse to switch the reference bistable on.

Integrator Offset Gate

This gate detects when the applied signal voltage is to be switched off and the offset voltage applied to the integrator.

Integrator Start Gate

This gate determines the start of the input voltage to the integrator and the beginning of the count of 10,000 pulses.

Signal Pulse Selector

This "and" gate feeds the 500Kc/s pulses into the counter during the period in which the input voltage is applied to the integrator.

Offset and Reference Pulse Selector

This "and" gate feeds the 1mc/s pulses into the counter during the period in which the offset or reference voltages are being applied to the integrator.

Reset Pulse Selector

This detects the time at which the resetting of the counters takes place.

Centre Strobe Start Gate

This detects when the counters have counted 9,900 pulses, i.e. when the counter reaches 18900.

Early Strobe Selector

This detects the point in which the early strobe for the split gate control loop is needed.

Early and Late Strobe Gates

These gates are used to produce the error signal for the oscillator control loop.

Start Pulse Gate

This gate lets an interrogate input signal into the programming unit.

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Transfer Store Output Gate

This detects when the programming unit is ready to permit a pulse to transfer the store onto the counter.

Printer Pulse Gate

This produces a waveform to the printer, to print the data at the appropriate time.

Complement Gate

When the zero detector is maladjusted this gate prevents the complement showing at the origin.

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## GROUNDED LOGIC

### List of Monostable used on DVM type 301-A

Centre Strobe Monostable

This is used to produce a waveform for the centre strobe.

Late Strobe Monostable

This is used to produce a waveform for the late strobe gate.

Delay Reset Monostable

This produces a delay during which the store transfer takes place.

Start and Early Strobe Monostable

The trailing edge is used to trip the integrator start gate and the interval defines the length of the early strobe.

Reset Pulse Former

This provides a suitable waveform of short duration to the counters to reset them to read 09000.

Transfer Store Pulse Transformer

This consists of a monostable and a delay circuit, each of which provides suitable waveforms to the counters for transferring to the store.

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# GROUNDED LOGIC

## List of Bistables used on DVM type 301-A

### Signal Bistable

This defines the signal period when the 500kc/s pulses are fed into the counters. When reset it provides a waveform for feeding the 1Mc/s pulses into the counters. This bistable is connected to the floating bistable so that they are operated in parallel.

### Integrator Bistable

This provides the complete operating period of the counters.

### 500Kc/s Bistable

This produces 500Kc/s by dividing the 1Mc/s clock frequency by two.

### Overload Bistable

This provides a waveform to drive the overload indicator neon at a low frequency.

### Selector Gating Bistable

This is used to select alternate waveforms from various monostables triggered by the mains Schmitt trigger.

### Read-out Bistables

These bistables produce waveforms of different periods for the transfer store pulse former.

### Start Pulse Store

This stores the interrogate input signal.

### Auxiliary Store

This stores a state for the transfer store pulse former.

### Printer Pulse Former

When there is a transfer store pulse, this stores the information until the mains Schmitt trigger changes its polarity.

### Schmitt Trigger

### Mains Schmitt Trigger

This provides a square waveform from the mains.

# FLOATING LOGIC

## Bistable A

This bistable defines the period when the input signal is applied to the integrating amplifier.

## Bistable B

This covers the complete operating period of the integrating amplifier.

## Schmitt Trigger and "Or" Gate

This provides a DC level indicating the polarity of the input and a zero crossing pulse whenever the integrator output goes through zero in either direction.

## "And" Gate F

This ensures that a zero crossing or F pulse is only provided during the reference period.

## "And" Gates C and D

These control the application of the positive and negative reference voltages respectively.

## Reference Bistable

This controls the time of application of the reference voltage.

## Positive and Negative Offset "And" Gates

These control the polarity and time of application of the offset voltage and apply "sign" information to the grounded logic.

Logical System

This description should be read in conjunction with the logical diagram of Fig.6. The diagram shows all the gates, monostables and bistables used together with blocks representing the decade counters.

The parts of the unit which are floating are shown in the top left hand corner enclosed by the dotted lines, all the couplings to this unit being made by transformers.

As mentioned previously the system used is worked synchronously with the mains frequency, the initiation of the measuring cycle being determined by a Schmitt trigger circuit working from the mains, this Schmitt trigger is on the left of the diagram near the bottom with the mains waveform (1) driving it.

Before the integration period commences the data in the counter is transferred to the store and the counter is reset to 09000. The transference of data to the store is carried out at a rate as set by the front panel controls, these controls choose a frequency from a binary dividing chain formed by bistables G H I J K and L. Waveform 2 from the Schmitt trigger is used to trigger bistable G and hence determine the transfer to store via the "read-out period" switch, the "Trigger" switch, the "read-out" switch and the "Transfer to store" pulse former L1 L2.

A delay before resetting the counter is provided by monostable A which is triggered directly from the mains Schmitt trigger circuit. This monostable is 1M sec. approximately. Since the reset is required on only alternate mains cycles this waveform is fed via the "Reset pulse selector" gate to the "Reset pulse former", waveforms (26) and (27). The reset pulse waveform is also used to reset the Start pulse store bistable in the "Programming Unit" which will be described later.

So far we have seen how the mains waveform is used to transfer the counter data to the store and reset the counter ready for the start of the signal integration period. Monostable B provides a delay after the reset before the commencement of the integration period. On alternate cycles the trailing edge of B is used to initiate the integration and switch in the oscillator pulses to the counter on the other alternate cycles waveform B is used as the early strobe in the oscillator control loop.

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The initiation of the integration is carried out by triggering bistables A and B via the integration start gate G waveform (7), the other inputs to this gate are bistable G at 25 c.p.s. and the 500Kc.p.s. pulses to prevent pulse splitting by the gates.

The use of waveform B in the oscillator control loop is via the early strobe selector which has a waveform G as its other input at 25 c.p.s.

Leaving the description of the oscillator control loop until later we will follow the action of bistables A and B, which have both been set by the trailing edge of monostable B waveform on alternate cycles of the mains. Bistable A determines the time that the signal is applied to the integrator via the floating bistable A. (The floating bistables A and B are worked in synchronism with the grounded bistables via the transformer couplings).

Bistable A is switched off when 10,000 pulses at 10,000 times the mains frequency have been fed into the counter and since the counter was initially set to 09000 this will be when it reads 19000, the gate which detects this is the integrator offset gate (since it initiates the offset period), it is shown above the counter, waveform (9). During the time that A and B are set, pulses from the 500K c.p.s., divide by two from the oscillator, are fed into the counter and the signal is fed into the integrator. In the floating unit switch A is open, B is closed, C and D are closed and the positive and negative offset gates are closed.

The next period following the signal integration period is the offset period. During this time which is 970 microseconds, a voltage of the same sign as the input signal is applied to the integrator input. The correct sign to apply is determined by the sign of the output of the zero detector at the end of the integration period, the voltage is applied by opening either the positive or negative offset switch. The logic for determining the appropriate time and sign is carried out by the positive and negative offset gates. The output from the positive or negative offset gates depends upon - not R X not A X B X Sign, (from the Schmitt trigger following the floating zero detector). These inputs ensure that the offset period follows the signal period for 970 pulses of the 1M c.p.s. oscillator and that the sign of the applied offset is the same as the input signal, the magnitude of the offset is adjusted so that the current into the integrator applied for 970 microseconds corresponds to the application of the reference waveform for 30 pulses at 1M c.p.s.

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The termination of the offset period and the start of the reference period are determined by a pulse from the counter when it reaches a count of 19970 this pulse is obtained from the integrator discharge gate O which is above the counter, waveform (10), it is used to set bistable R which is reset by the zero detector pulse when the integrator output passes through zero, this pulse also resets bistable B (grounded and floating).

The working of the oscillator control loop has been described earlier, the necessary early pulse depending on the counter is obtained from the counter gate N, and is used for initiating the centre strobe monostable which is gated in the control loop with the early strobe obtained from monostable B, and the late strobe obtained from the late strobe monostable which is triggered by the trailing edge of the early strobe, the error signal obtained is passed via an amplifier and integrator to control and oscillator.

Programming Unit

The programming unit is formed by the Start pulse store and Ancillary store bistables, the Printer pulse former and the gates J, K and L. The need for the store arises since the interrogate pulse may be presented in the middle of a measuring period. On receiving an interrogate pulse the "Start pulse store" bistable is set and holds the interrogation information until the DVM is ready to make use of it which is after the reset pulse. When the reset pulse occurs the "Start pulse store" bistable is reset by the auxiliary store bistable which retains the interrogation information during the measuring period, (on NPL type, "start pulse store" retains the information till following G), this bistable being reset by the subsequent transfer to store pulse G. The waveforms are shown in Fig. 4.

Input Amplifier and Integrator Circuits

The input and integrating amplifiers are identical chopper stabilized units. Referring to the circuit diagram (Fig.7 ) it can be seen that each amplifier is divided into two sections. The upper section is the main part of the amplifier which is AC coupled to the input terminal. DC and low frequency components are filtered off through the lower section which is a chopper amplifier. The combined frequency response gives a maximum gain at DC of $10^8$ falling to $10^5$ in a flat mid band region extending from 10cps to 1Kcps. Above 1Kcps the gain falls off at about 9 db per octave.

The chopper is a field effect transistor VT2. After amplification the chopped signal is demodulated by transistor VT12. This is followed by filter circuits which remove the chopper ripple. VT2 and VT12 are driven synchronously by the multivibrator circuit VT35 and VT37 at about 1Kcps., (VT35 and VT37 also drive the chopper is the integrator amplifier).

The high frequency and low frequency components are re-combined in the input stage of the amplifier which consists of VT1, 3, 6 and 10. The remaining stages provide wideband amplification incorporating the necessary frequency shaping. The output stage is a Class A emitter follower with a constant current transistor load.

The feedback circuits of the input amplifier are shown in simplified form in Fig.7.

It can be seen that current feedback is used to give a high input impedance, the value of which is given by the relation

$$Z_{in} = \frac{AR}{G}$$

where A is the open loop gain
R is the actual input resistance of the amplifier
G is the closed loop gain

The feedback resistors are set to give a gain of 2 on the 10V range so that the voltage measuring circuits operate over a scale of ± 20V. The maximum output of the amplifier is ± 30V to allow for 40% linear overranging.

Cont'd....

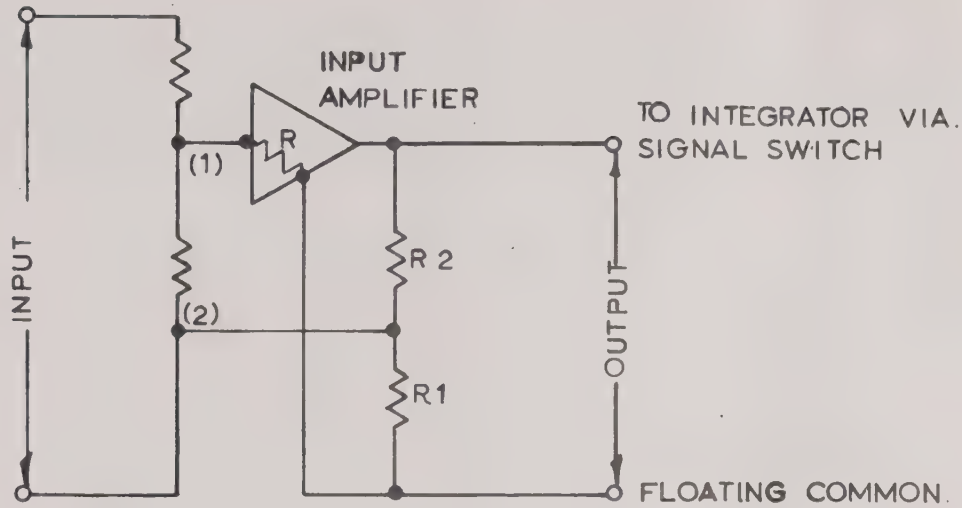
On the 1V and 100mV ranges the gain is increased to 20 and 200 respectively, whilst on the 100V and 1000V ranges attentuation of the input of 10:1 and 100:1 is provided.

The integrator amplifier is arranged to give an output of ± 20V when its input is held at ± 20V for the 20ms signal period. This is set by the values of R69, R70, R72 and C29A. The integrator is discharged by the reference voltage in 10ms max. through R129 and R129A or R130, R130 and RV8.

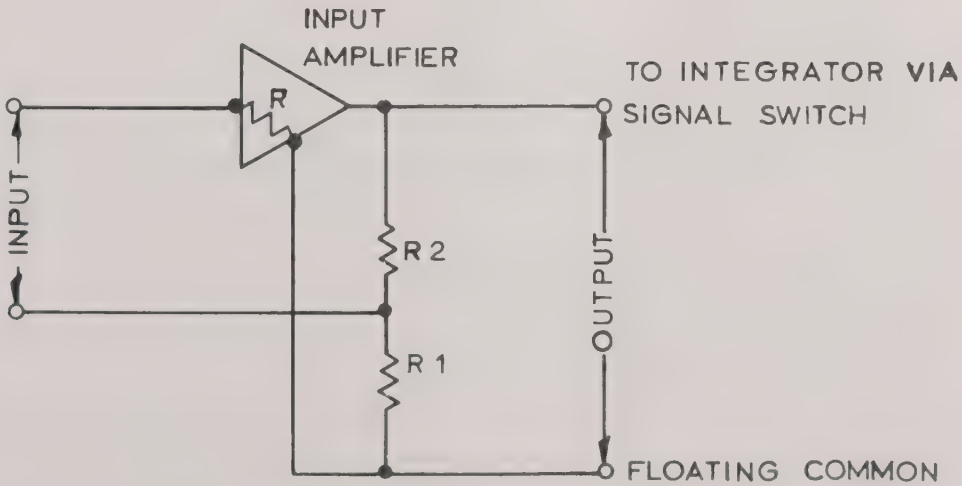
A small offset voltage is generated during the 970us preceding the discharge by applying a current through R131 or R132.

Both amplifiers have fast overload recovery circuits consisting of chains of zener and silicon diodes which apply maximum feedback if the output voltage exceeds ± 30V.

FIG 1



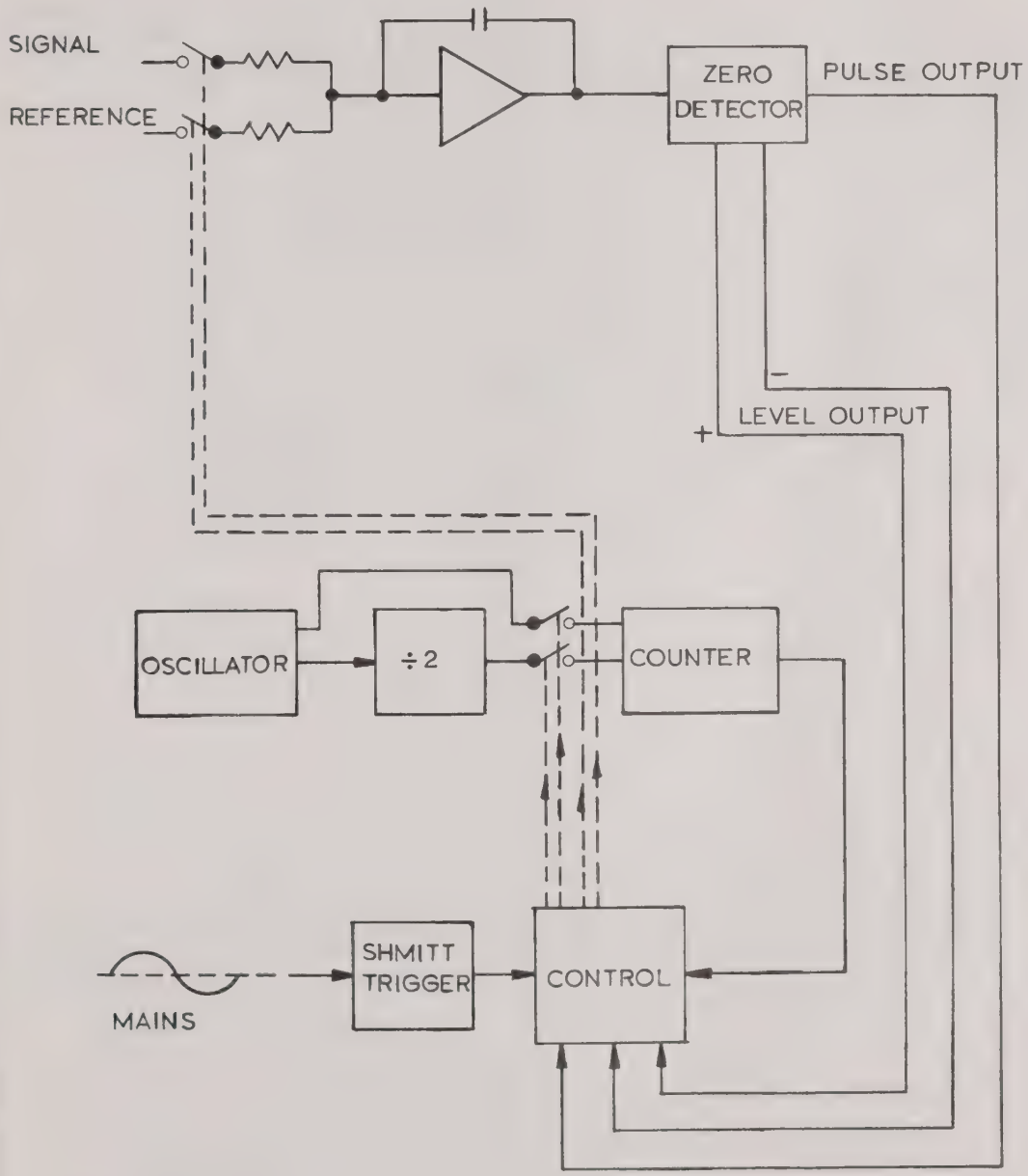

HIGH RANGES 100 V, 1000 V.




LOW RANGES 10V, 1 V, 100mV.

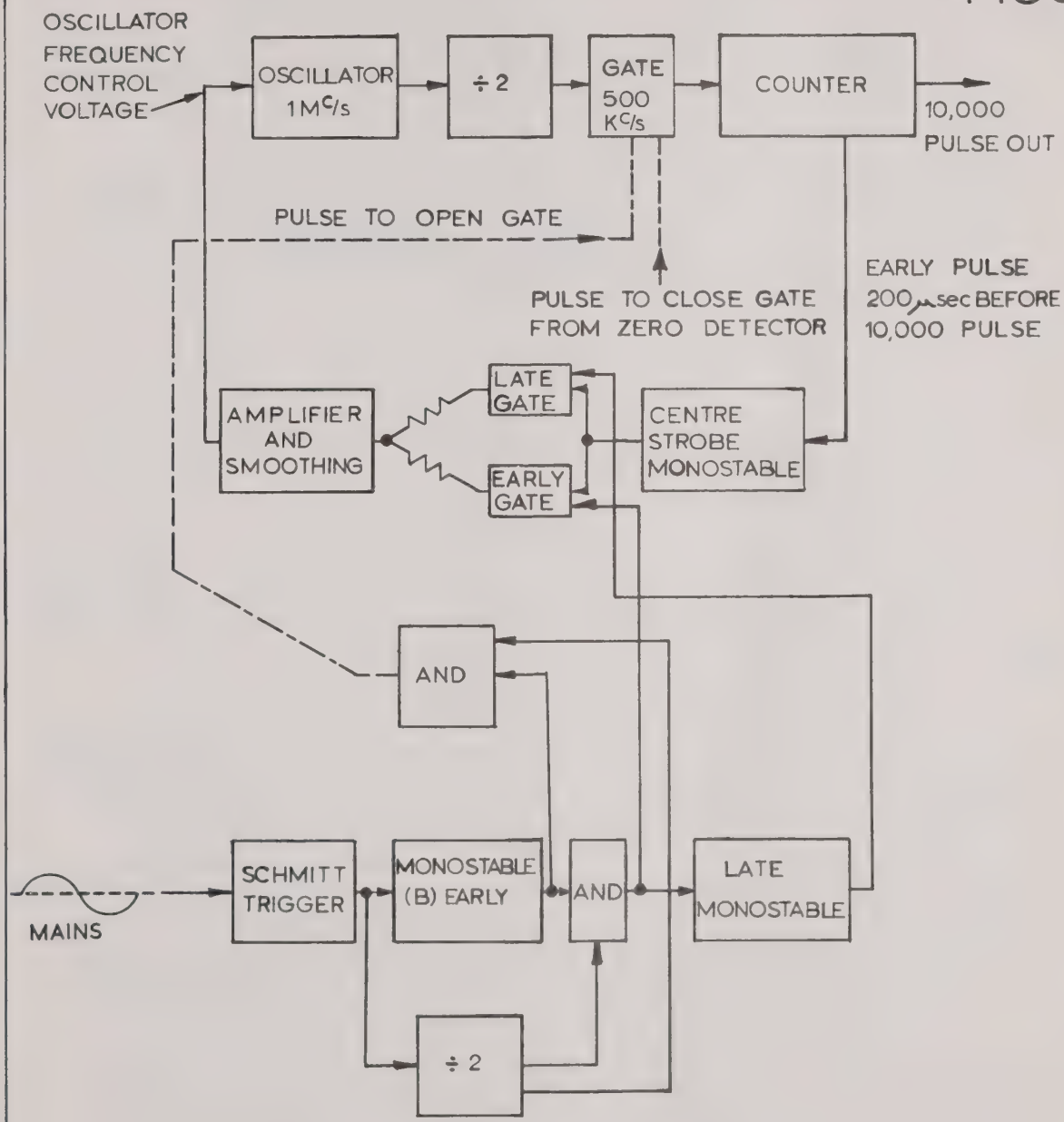
# INPUT AMPLIFIER

FIG 2



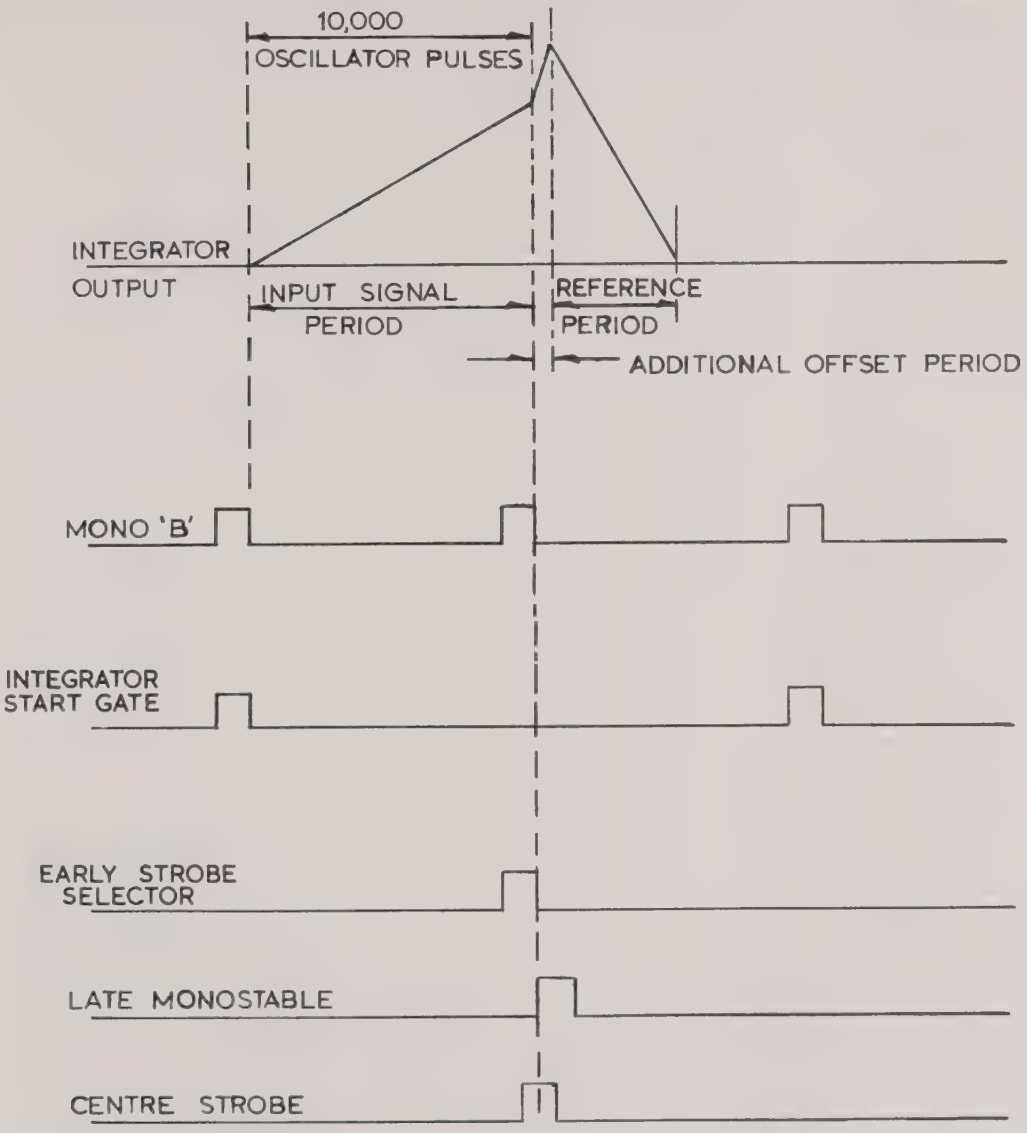

INTEGRATOR AND SWITCHING (GENERAL SCHEMATIC).

FIG 3

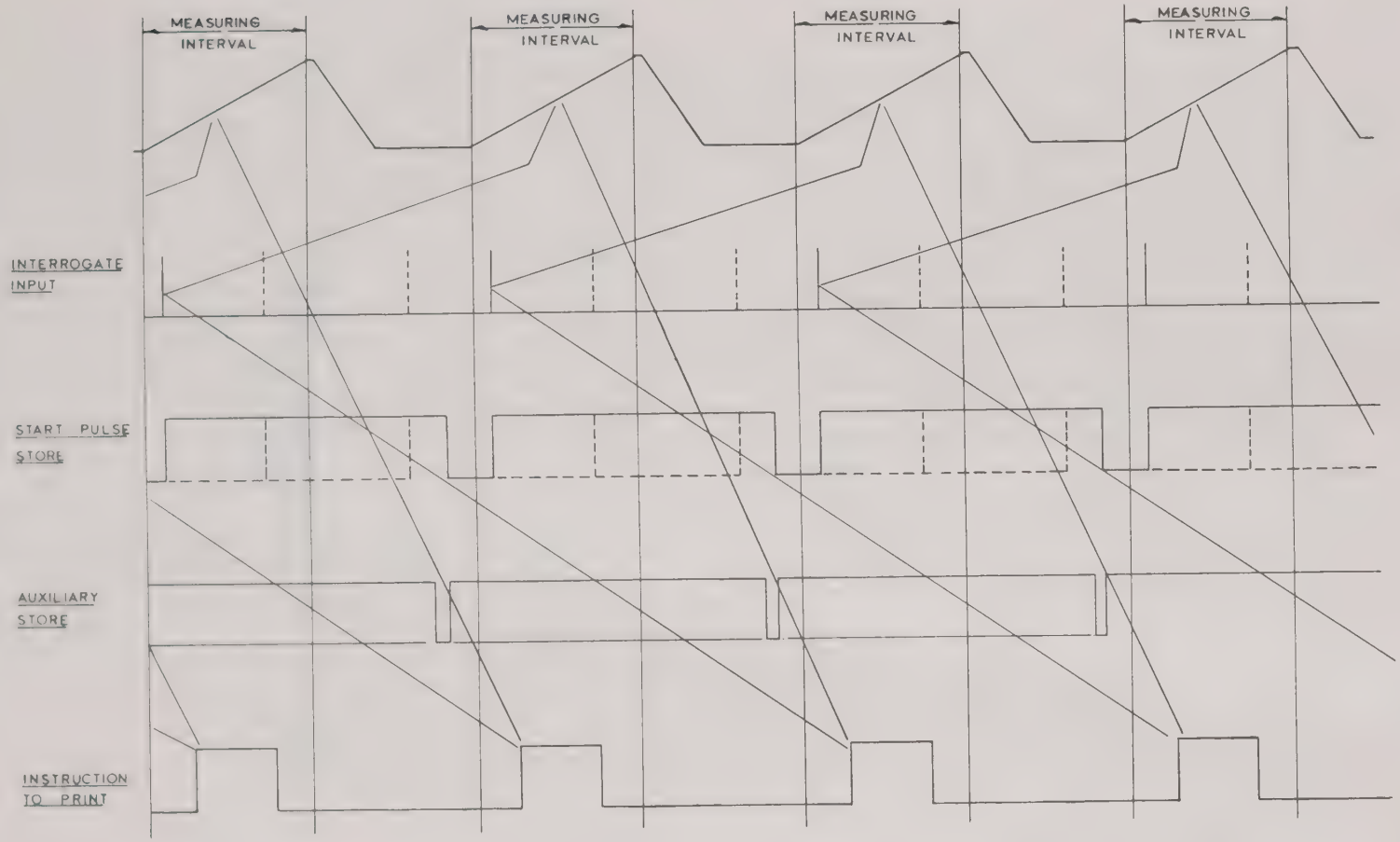



SYSTEM USED TO CONTROL THE INTEGRATION PERIOD.

FIG3a

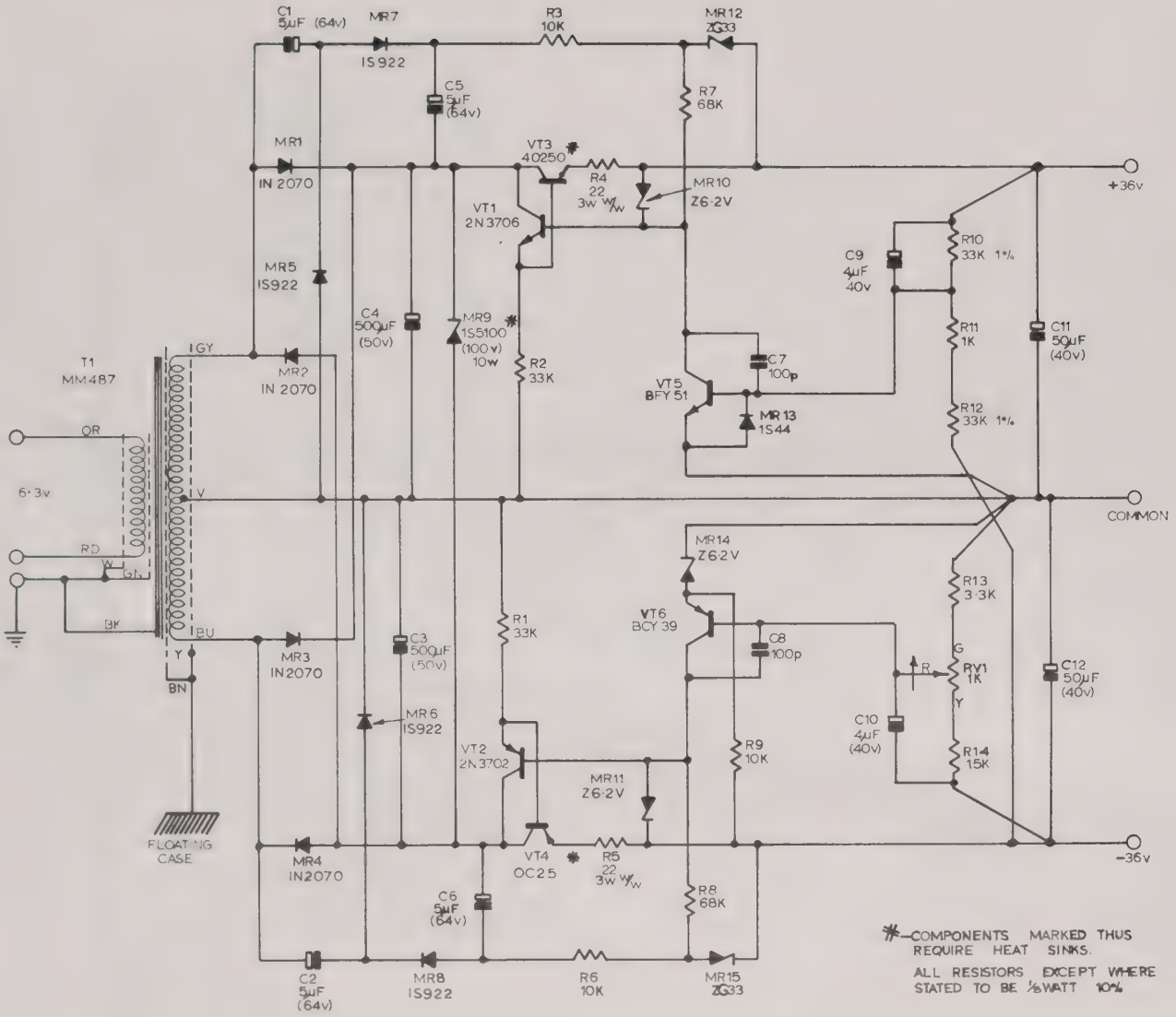



TIMING OF THE EARLY AND LATE STROBE LOCKING WAVEFORMS.

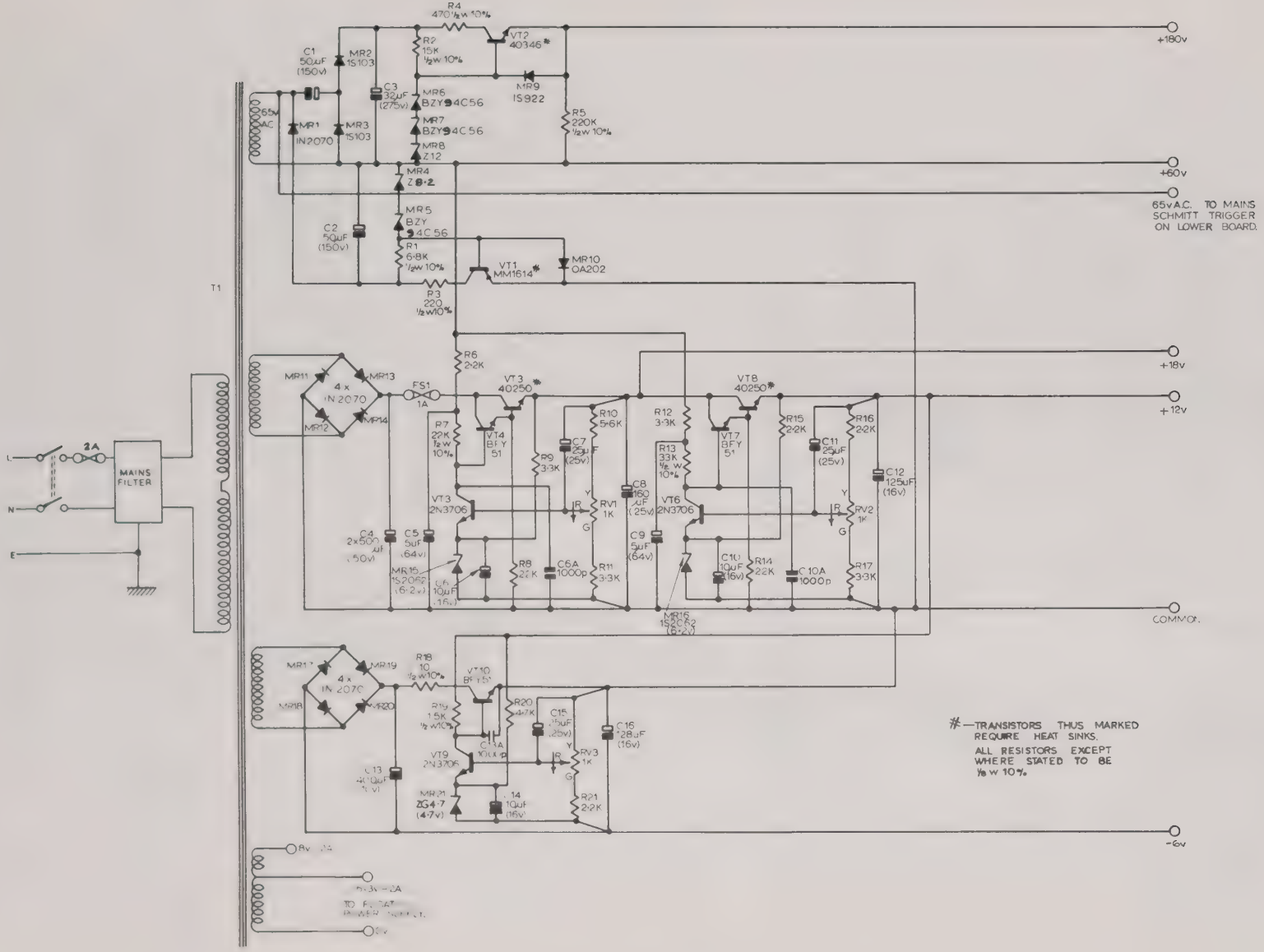



PROGRAMMING UNIT WAVE FORMS.

FIG 4




D.V.M. FLOATING POWER SUPPLY FIG.8.



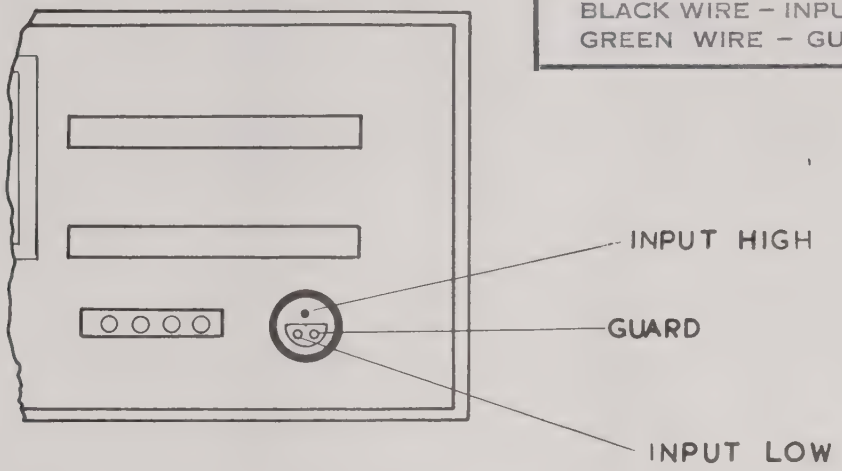

*—TRANSISTORS THUS MARKED REQUIRE HEAT SINKS.

ALL RESISTORS EXCEPT WHERE STATED TO BE ½w 10%

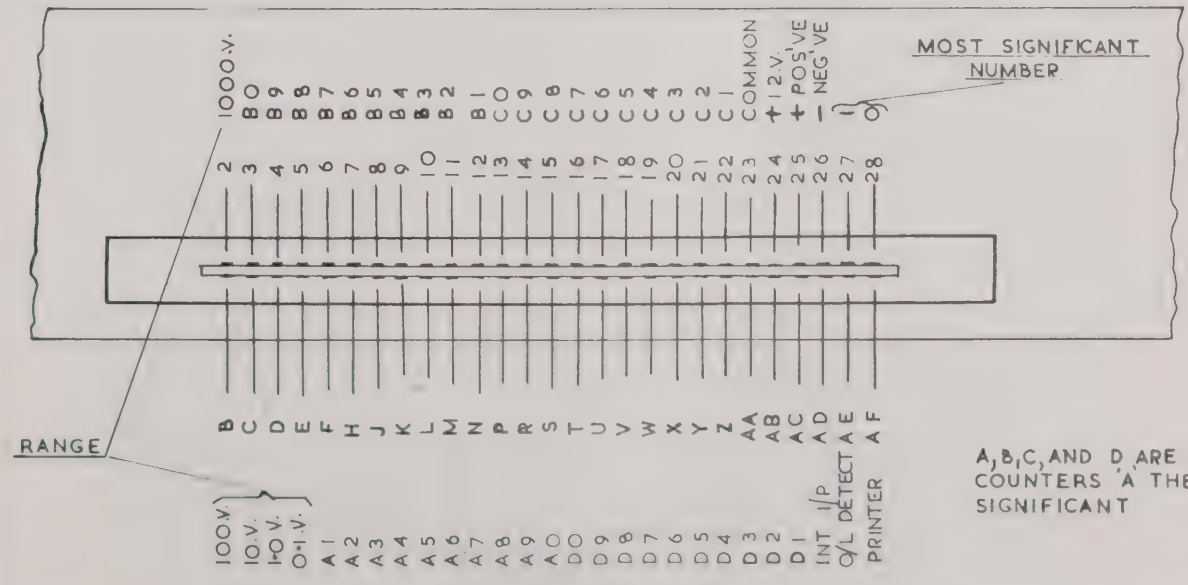
# DVM GROUNDED POWER SUPPLY

# FIG. 9

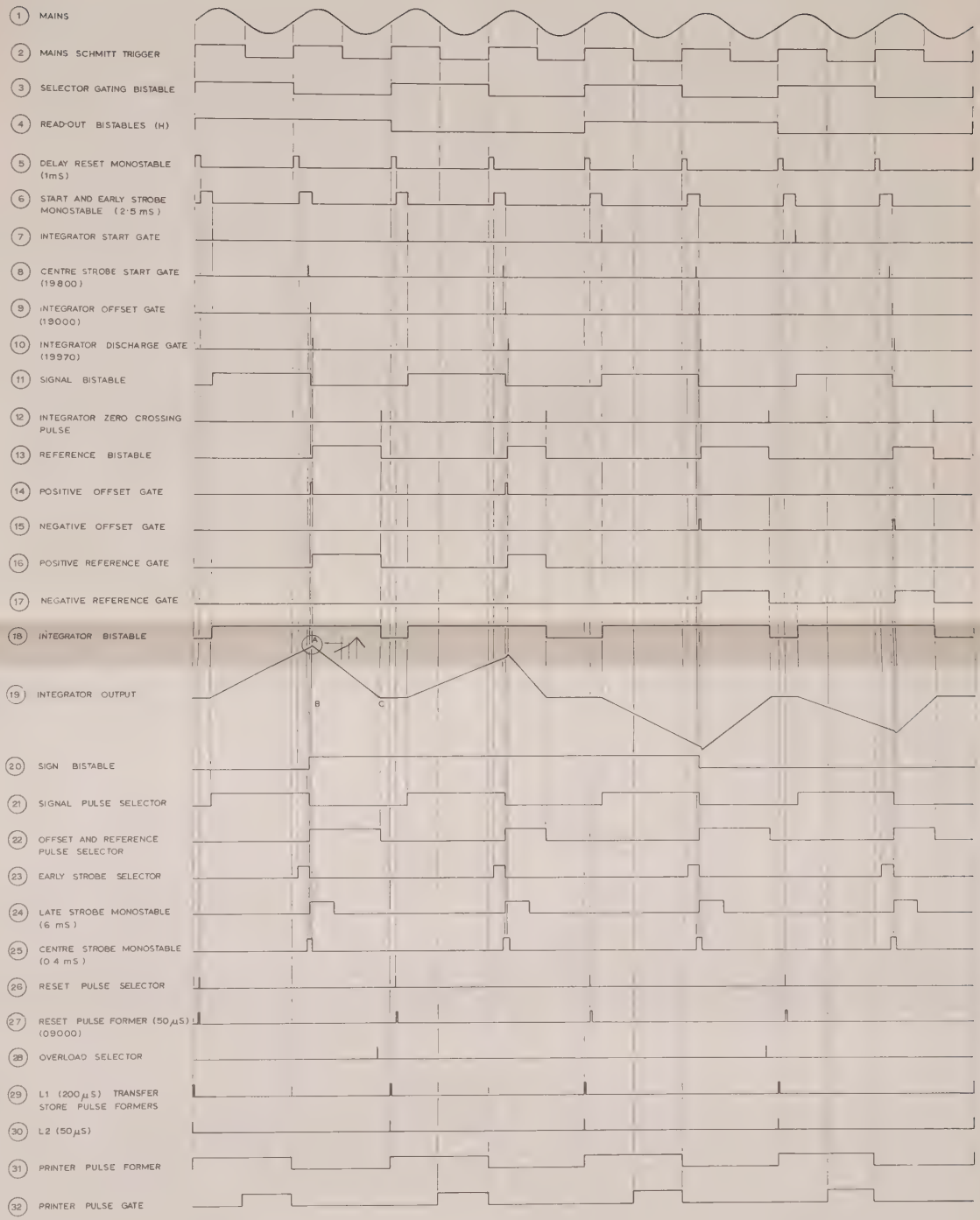
I/P LEAD CONNECTIONS
RED WIRE – INPUT HIGH
BLACK WIRE – INPUT LOW
GREEN WIRE – GUARD




## INPUT SOCKET CONNECTIONS

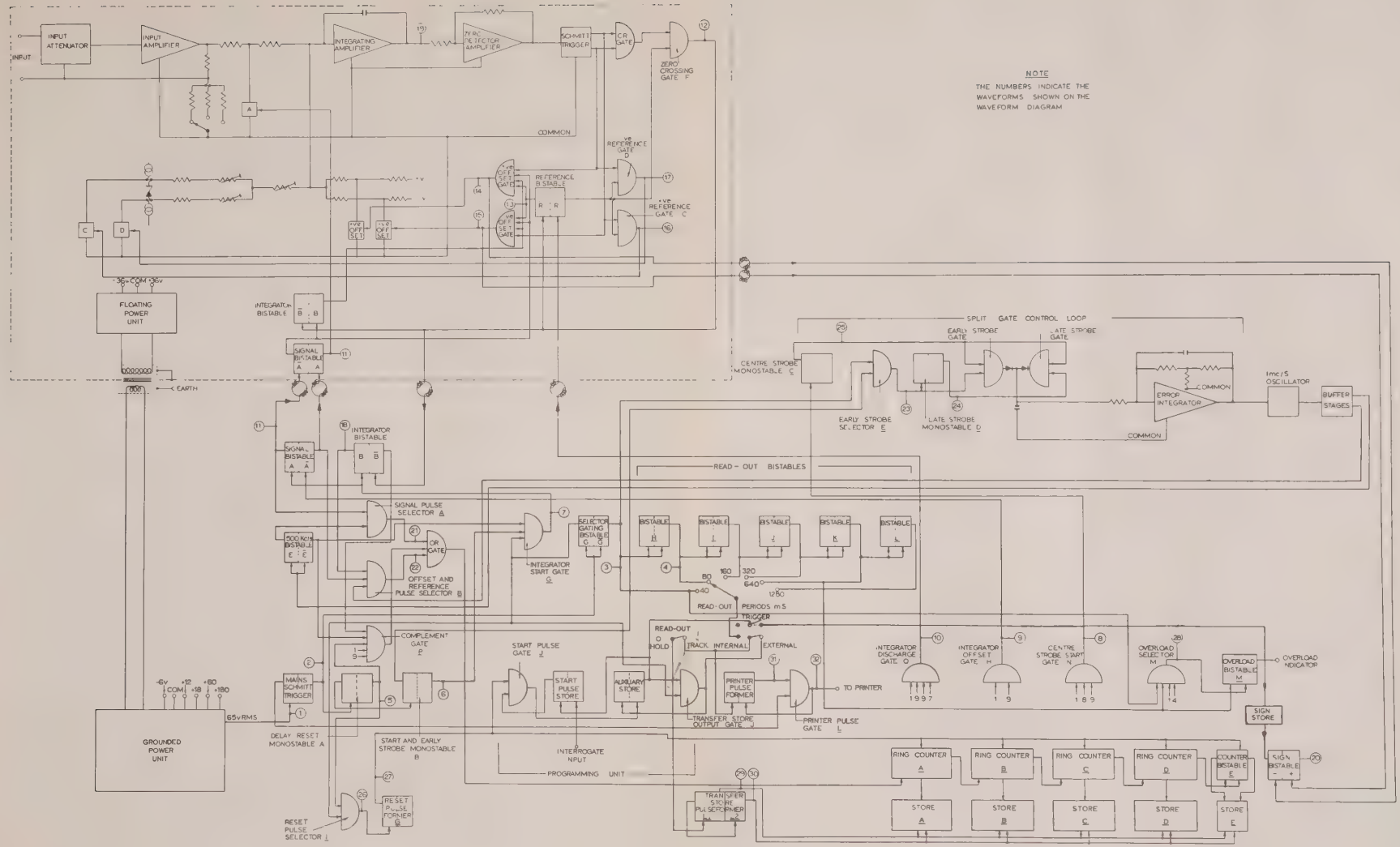

MOST SIGNIFICANT NUMBER
1000 V.
B0 B9 B8 B7 B6 B5 B4 B3 B2 B1 C0 C9 C8 C7 C6 C5 C4 C3 C2 C1
COMMON
+12 V.
+ POS VE
– NEG VE
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
RANGE
100 V.
10 V.
1-0 V.
0·1 V.
B C D E F H J K L M N P R S T U V W X Y Z AA AB AC AD AE AF
A1 A2 A3 A4 A5 A6 A7 A8 A9 A0 D0 D9 D8 D7 D6 D5 D4 D3 D2 D1
INT I/P
O/L DETECT
PRINTER
A, B, C, AND D ARE RING COUNTERS 'A' THE LEAST SIGNIFICANT

## OUTPUT PLUG CONNECTIONS


1 MAINS
2 MAINS SCHMITT TRIGGER
3 SELECTOR GATING BISTABLE
4 READ-OUT BISTABLES (H)
5 DELAY RESET MONOSTABLE (1mS)
6 START AND EARLY STROBE MONOSTABLE (2·5 mS)
7 INTEGRATOR START GATE
8 CENTRE STROBE START GATE (19800)
9 INTEGRATOR OFFSET GATE (19000)
10 INTEGRATOR DISCHARGE GATE (19970)
11 SIGNAL BISTABLE
12 INTEGRATOR ZERO CROSSING PULSE
13 REFERENCE BISTABLE
14 POSITIVE OFFSET GATE
15 NEGATIVE OFFSET GATE
16 POSITIVE REFERENCE GATE
17 NEGATIVE REFERENCE GATE
18 INTEGRATOR BISTABLE
19 INTEGRATOR OUTPUT
A
B
C
20 SIGN BISTABLE
21 SIGNAL PULSE SELECTOR
22 OFFSET AND REFERENCE PULSE SELECTOR
23 EARLY STROBE SELECTOR
24 LATE STROBE MONOSTABLE (6 mS)
25 CENTRE STROBE MONOSTABLE (0·4 mS)
26 RESET PULSE SELECTOR
27 RESET PULSE FORMER (50 μS) (09000)
28 OVERLOAD SELECTOR
29 L1 (200 μS) TRANSFER STORE PULSE FORMERS
30 L2 (50 μS)
31 PRINTER PULSE FORMER
32 PRINTER PULSE GATE

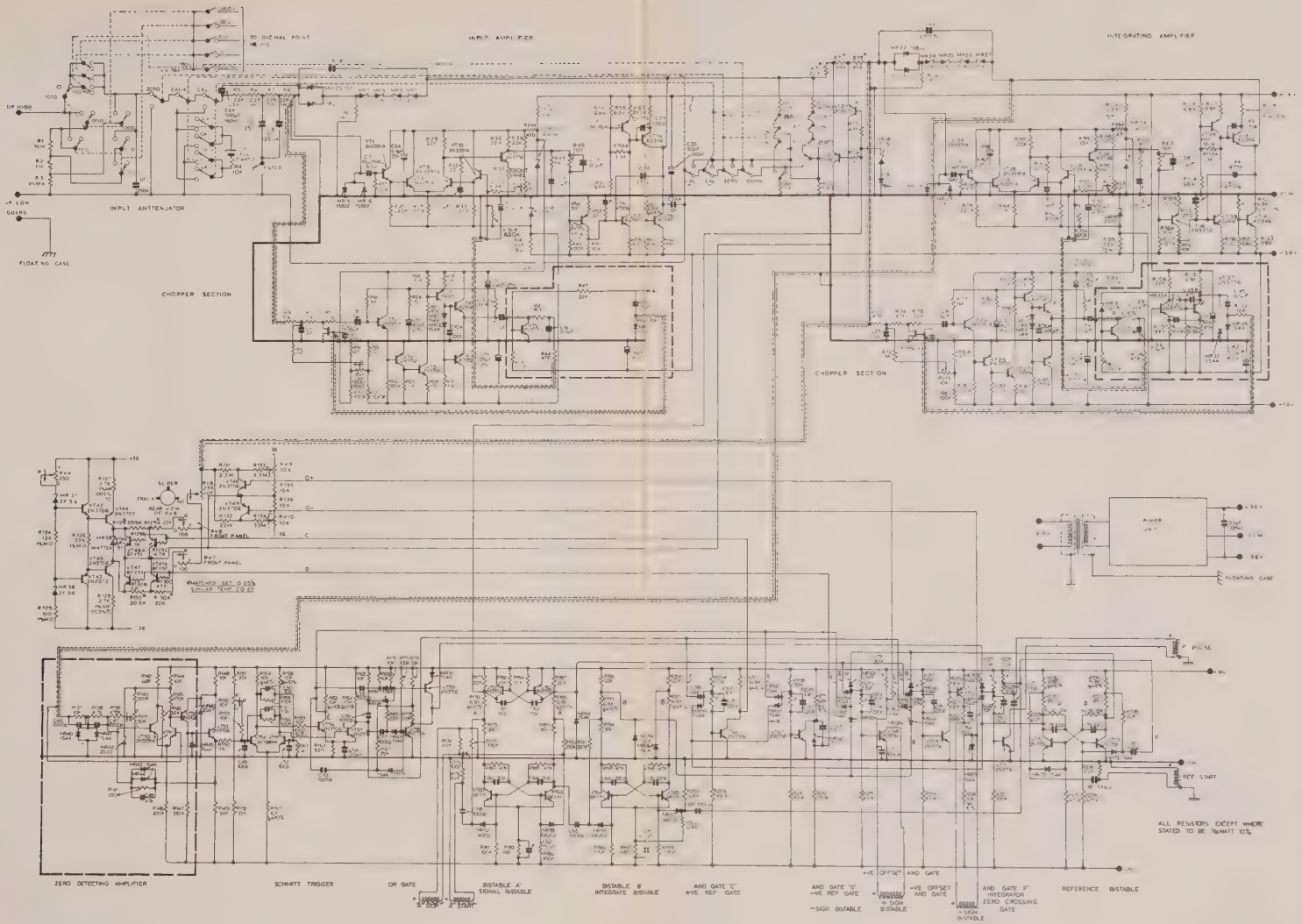
DVM WAVEFORM DIAGRAM

FIG 5

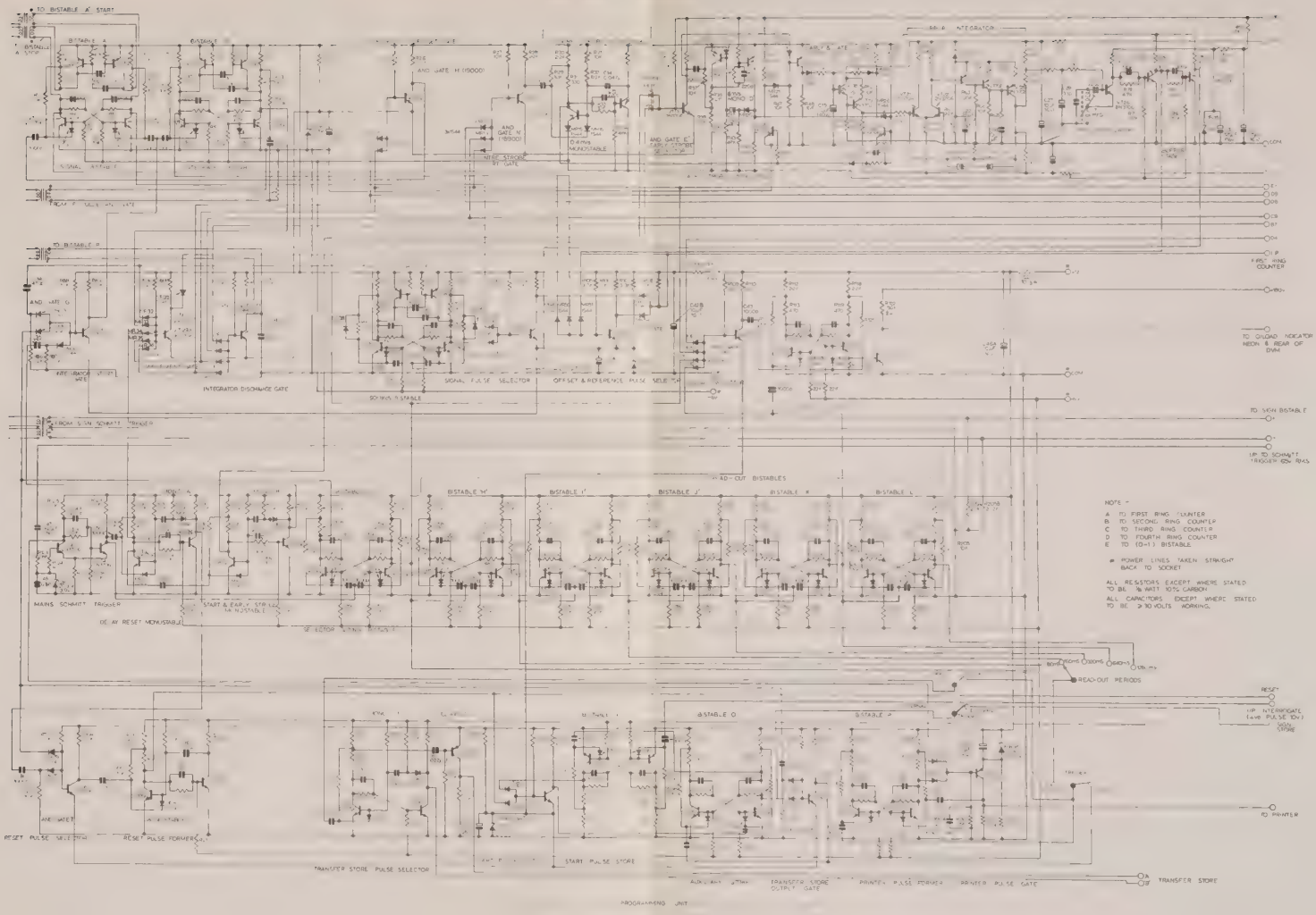



DVM BLOCK SCHEMATIC

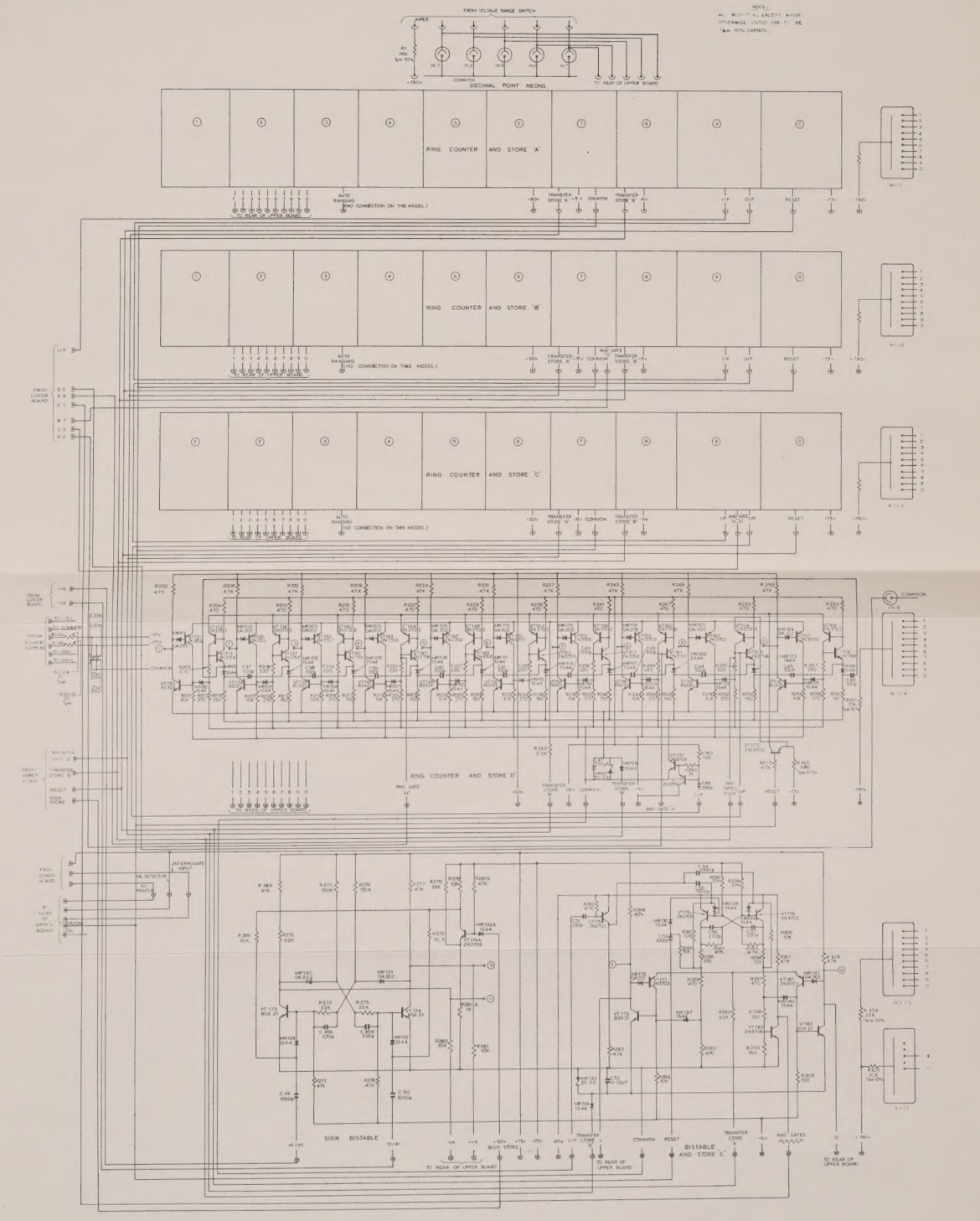
FIG6




DVM FLOATING UNIT
FIG 7.5.



DVM GROUNDED LOGIC
(Lower Board)
FIG 7b.




DVM COUNTERS

FIG 7c.